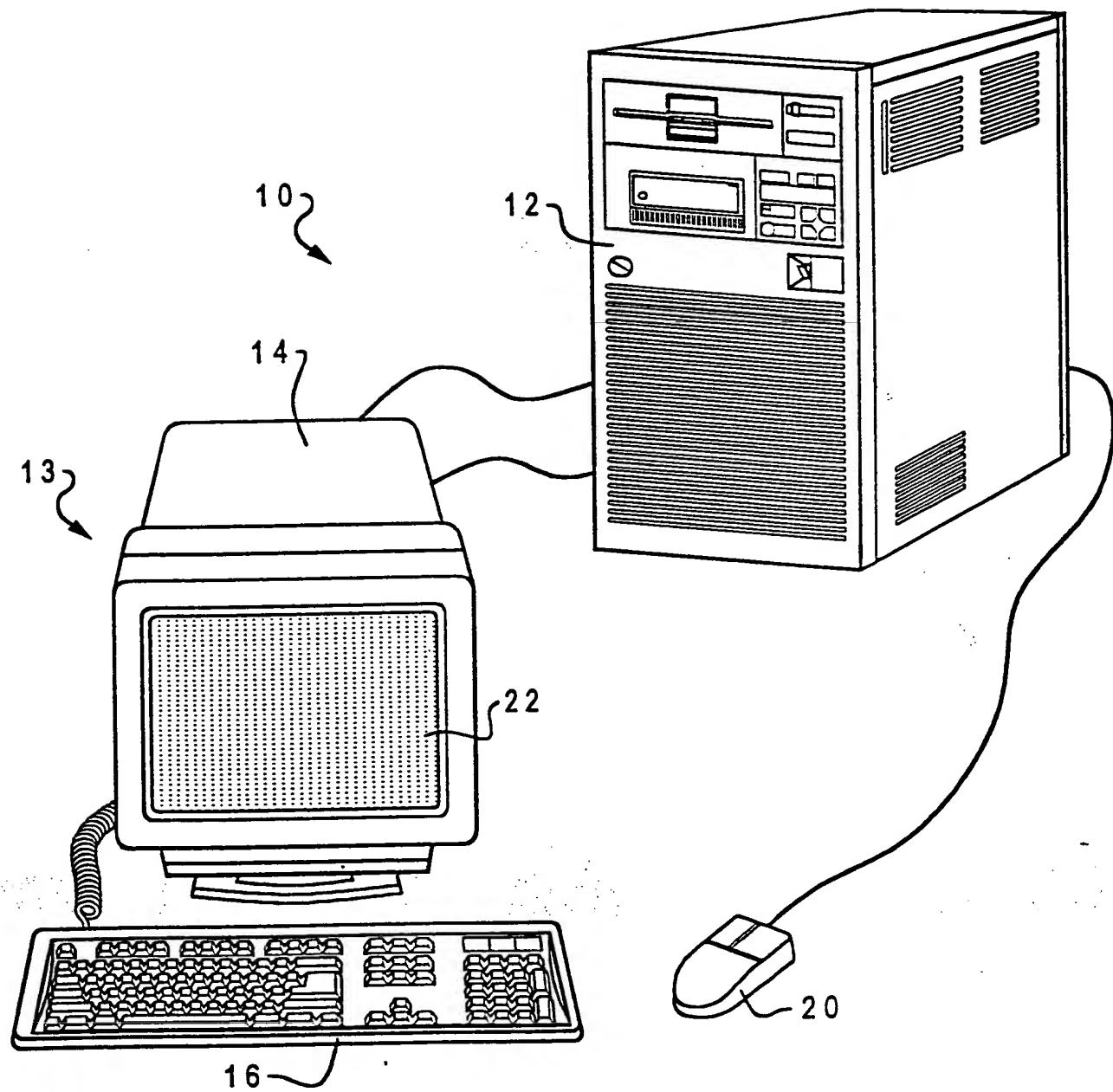


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*Fig. 1*

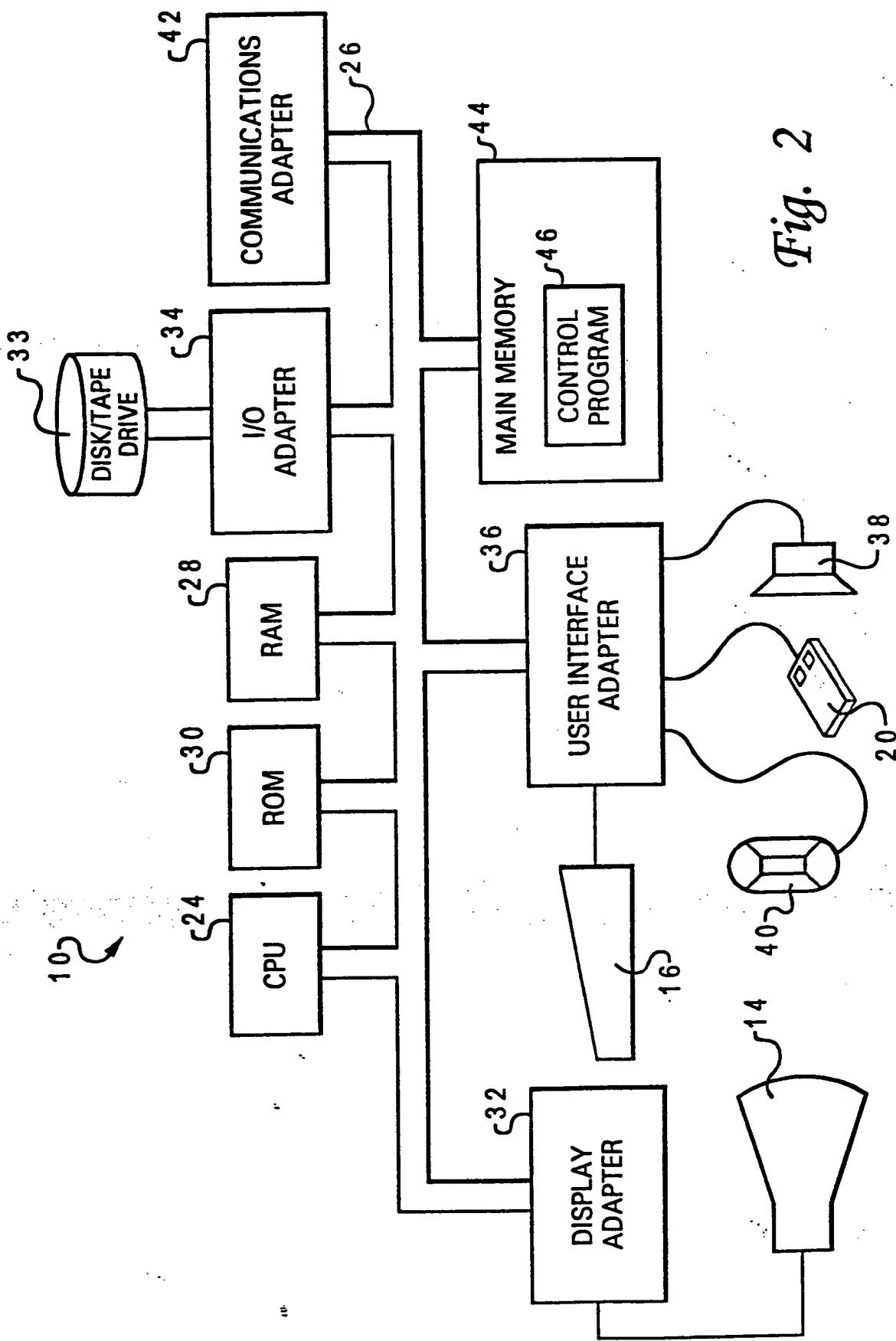


Fig. 2

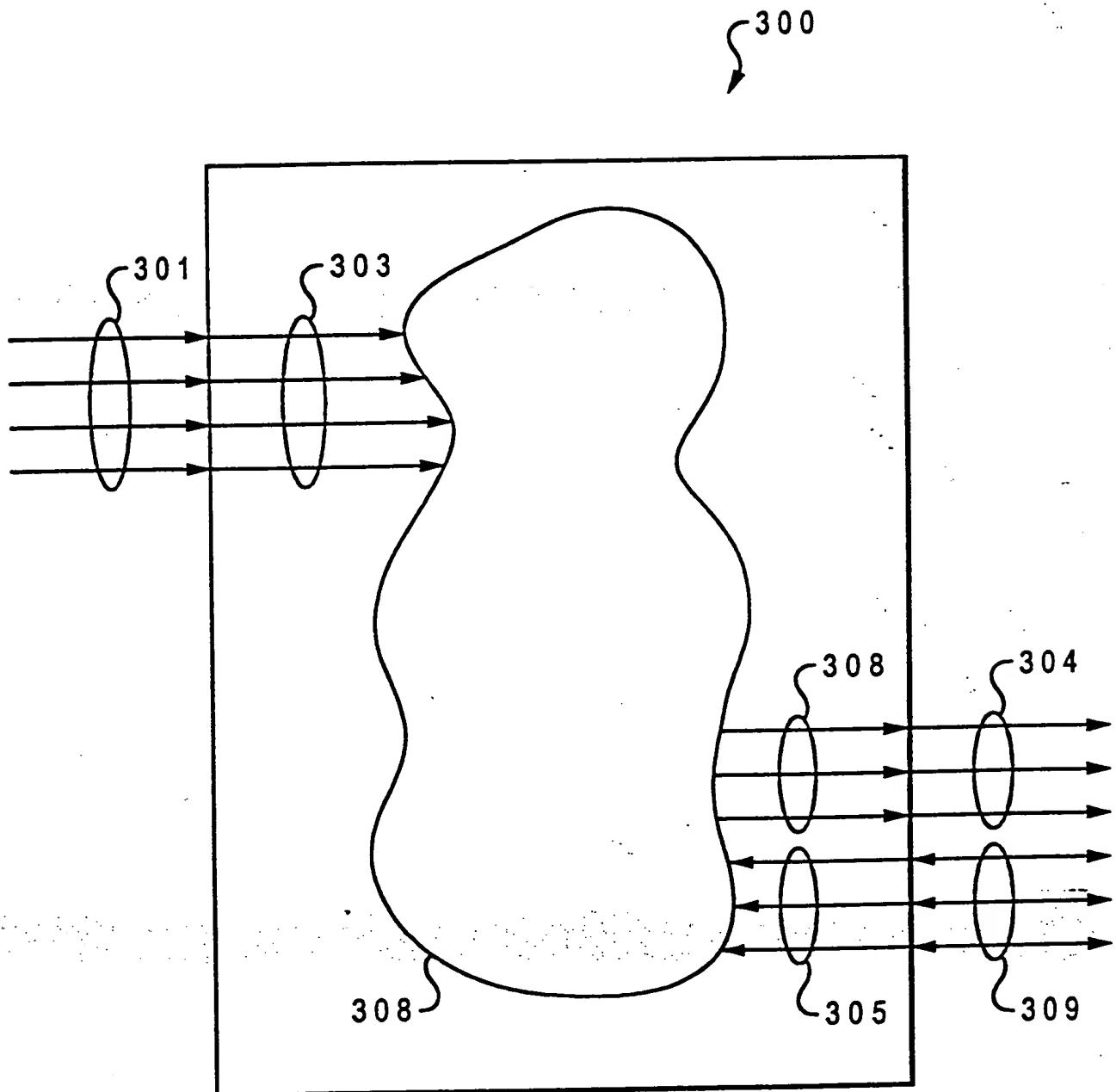


Fig. 3A

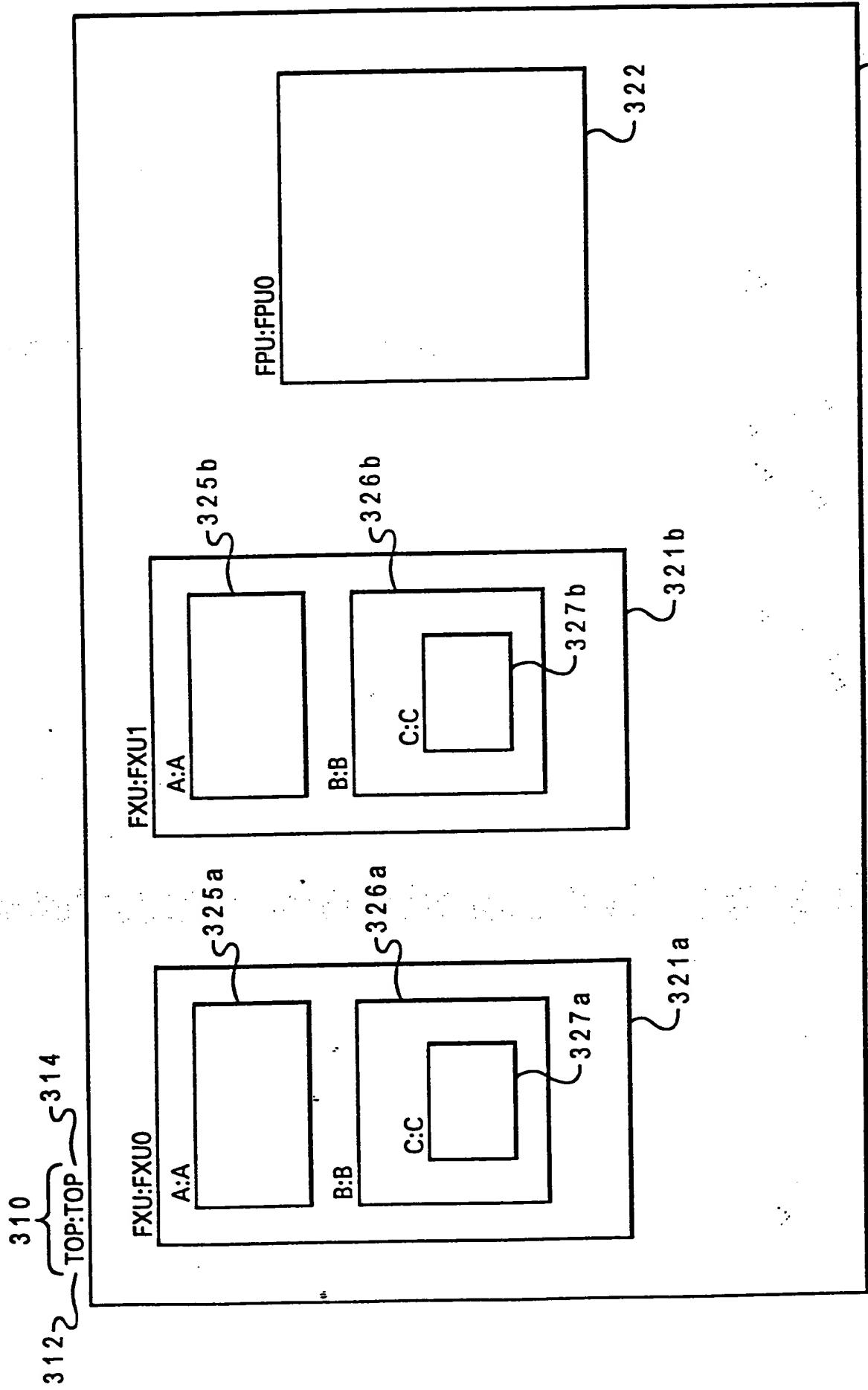


Fig. 3B

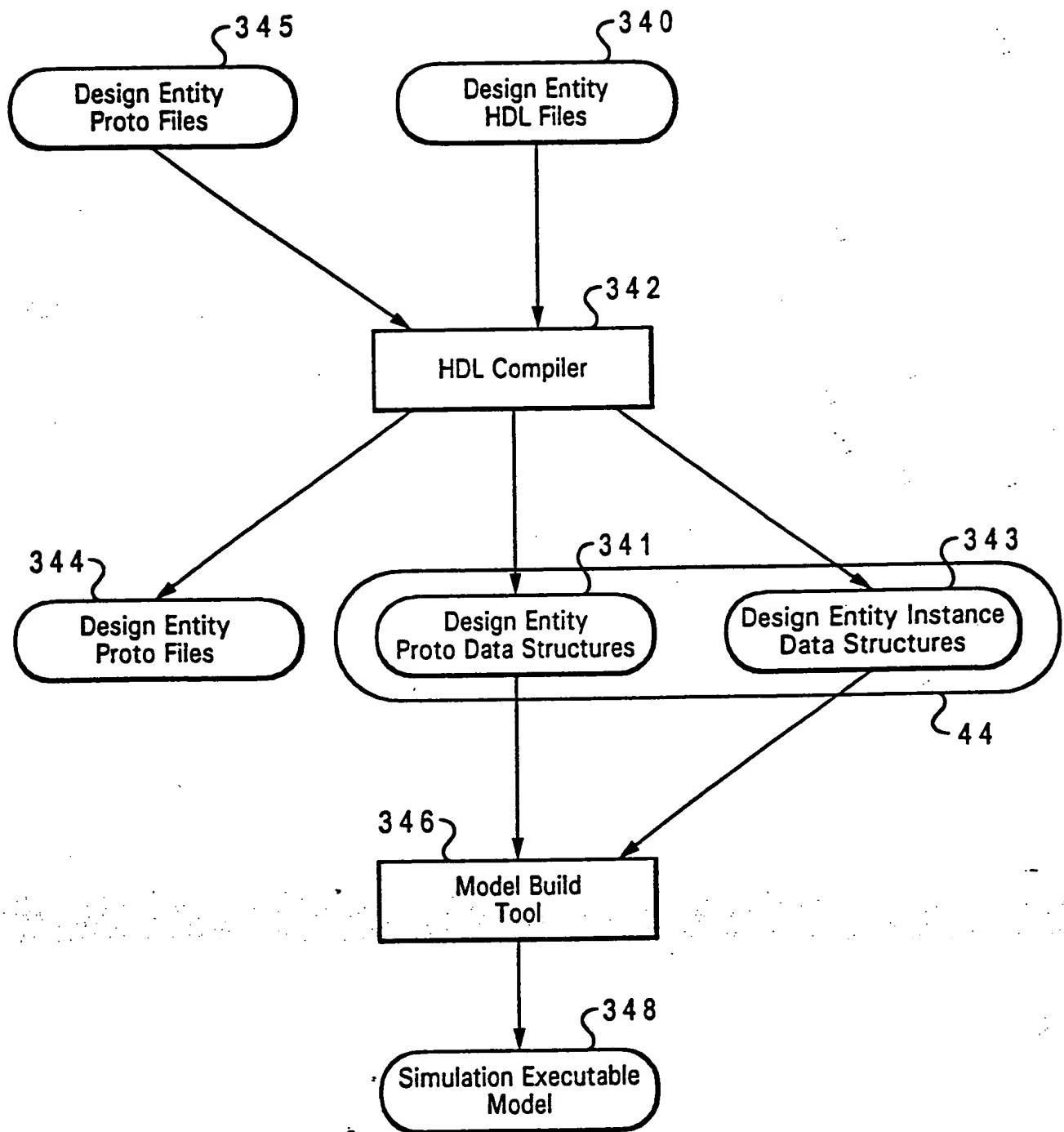


Fig. 3C

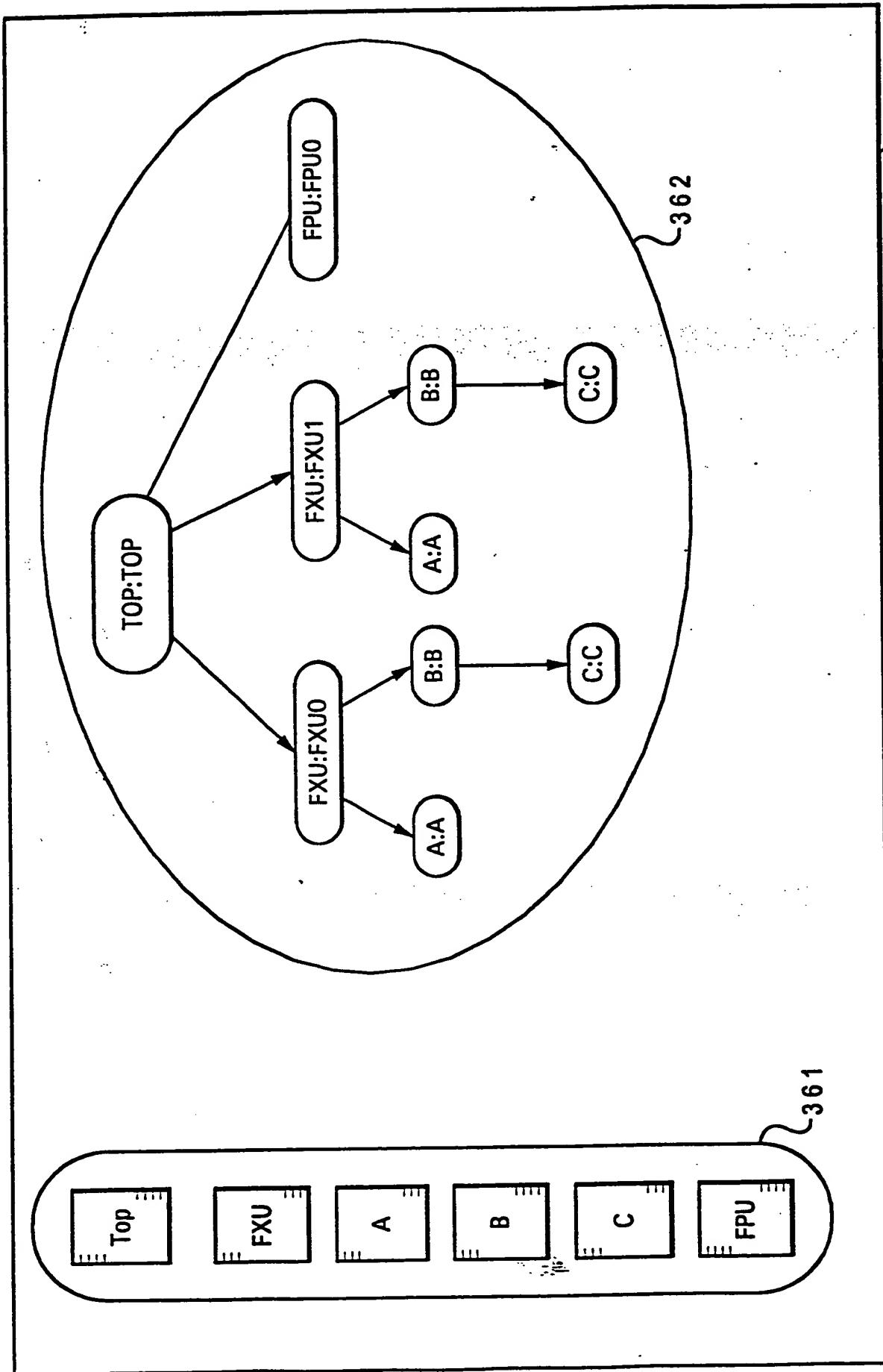


Fig. 3D

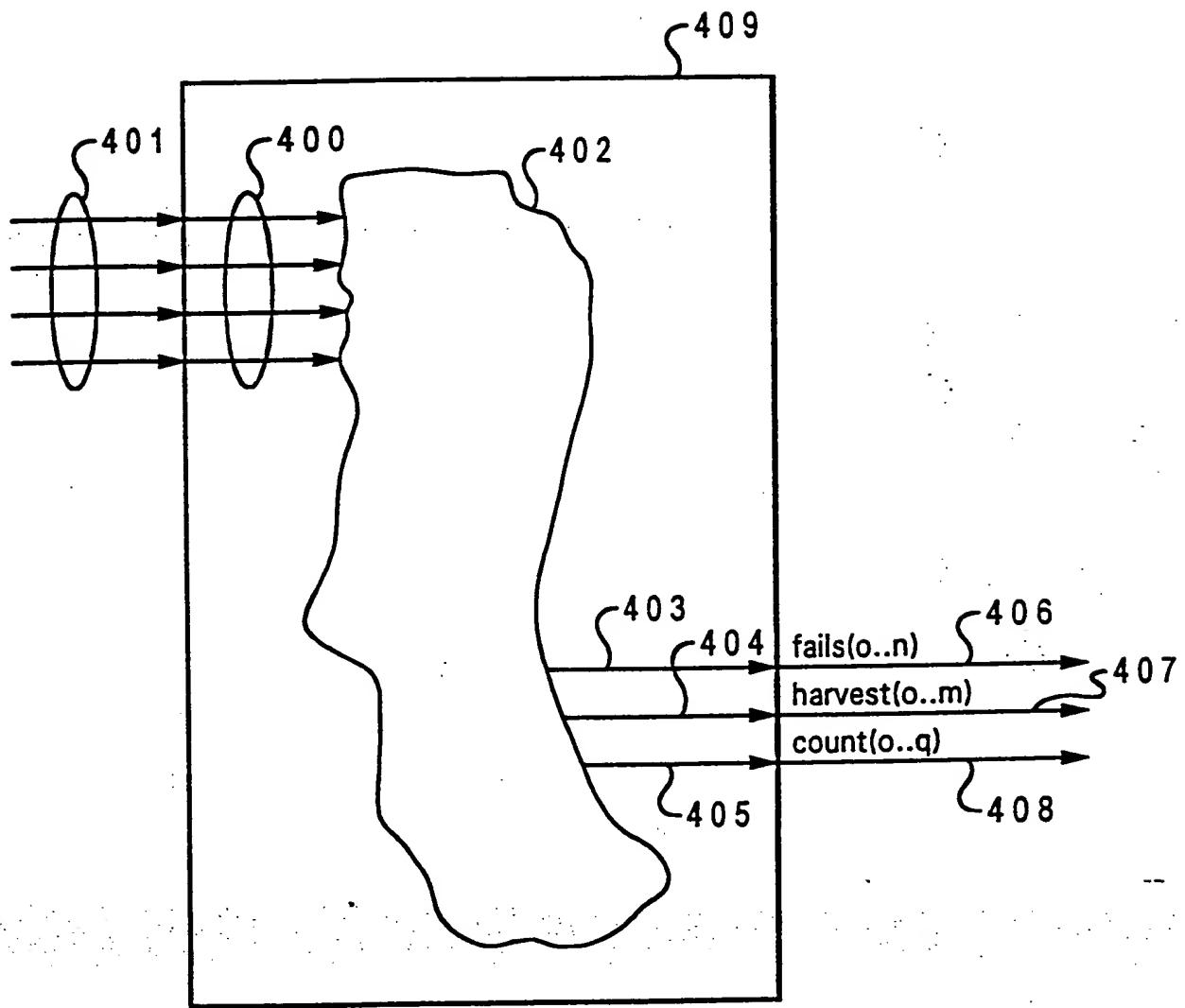


Fig. 4A

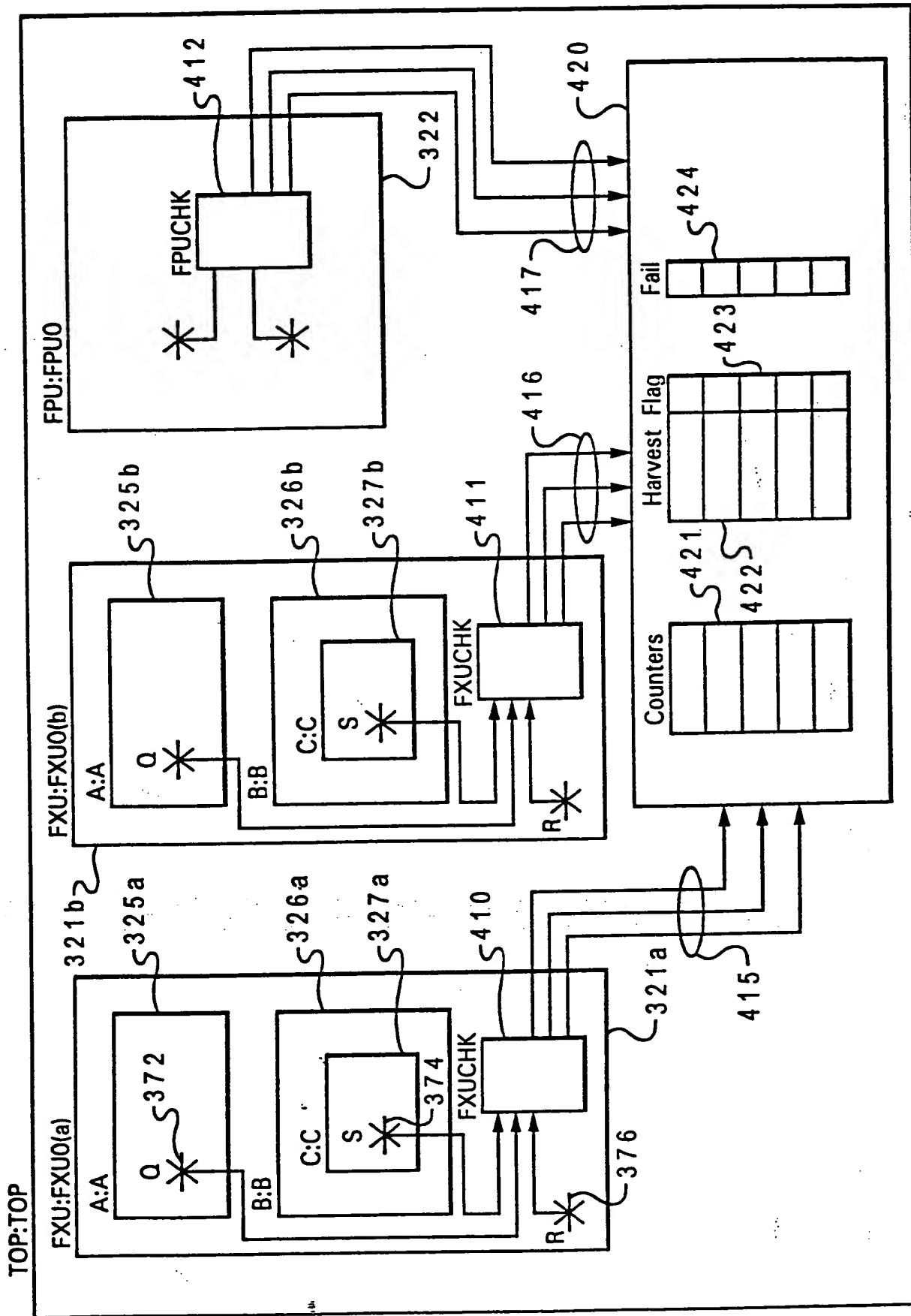


Fig. 4B

ENTITY FXUCHK IS

```
PORT( S_IN      : IN std_ulogic;
       Q_IN      : IN std_ulogic;
       R_IN      : IN std_ulogic;
       clock     : IN std_ulogic;
       fails     : OUT std_ulogic_vector(0 to 1);
       counts    : OUT std_ulogic_vector(0 to 2);
       harvests  : OUT std_ulogic_vector(0 to 1);
);
```

450

452 {  
-!! BEGIN  
-!! Design Entity: FXU;

453 {  
-!! Inputs  
-!! S\_IN => B.C.S;  
-!! Q\_IN => A.Q;  
-!! R\_IN => R;  
-!! CLOCK => clock;  
-!! End Inputs

454 {  
-!! Fail Outputs;  
-!! 0 : "Fail message for failure event 0";  
-!! 1 : "Fail message for failure event 1";  
-!! End Fail Outputs;

455 {  
-!! Count Outputs;  
-!! 0 : <event0> clock;  
-!! 1 : <event1> clock;  
-!! 2 : <event2> clock;  
-!! End Count Outputs;

456 {  
-!! Harvest Outputs;  
-!! 0 : "Message for harvest event 0";  
-!! 1 : "Message for harvest event 1";  
-!! End Harvest Outputs;

457 {  
-!! End;

440

451

ARCHITECTURE example of FXUCHK IS

BEGIN

... HDL code for entity body section ...

END;

458

Fig. 4C

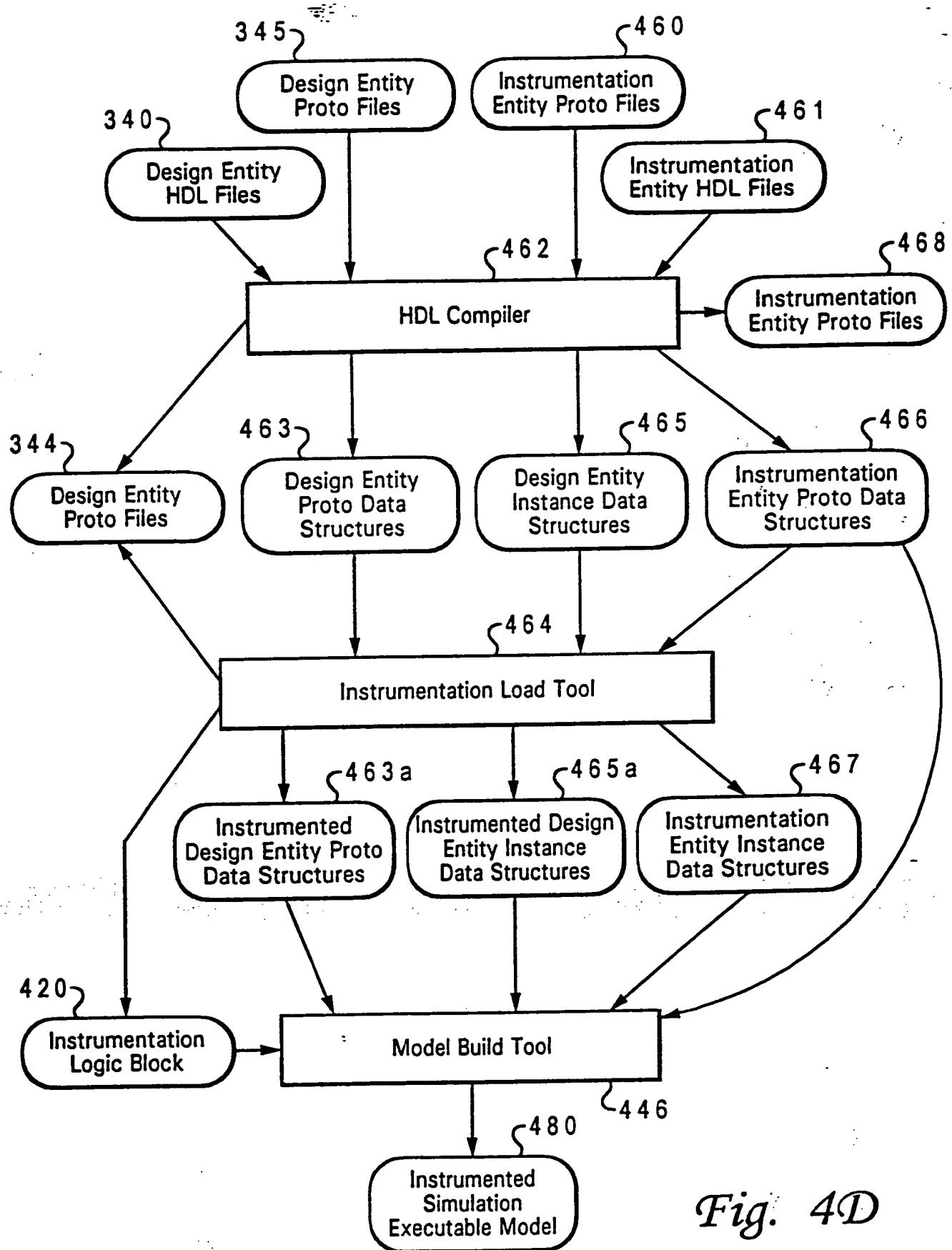


Fig. 4D

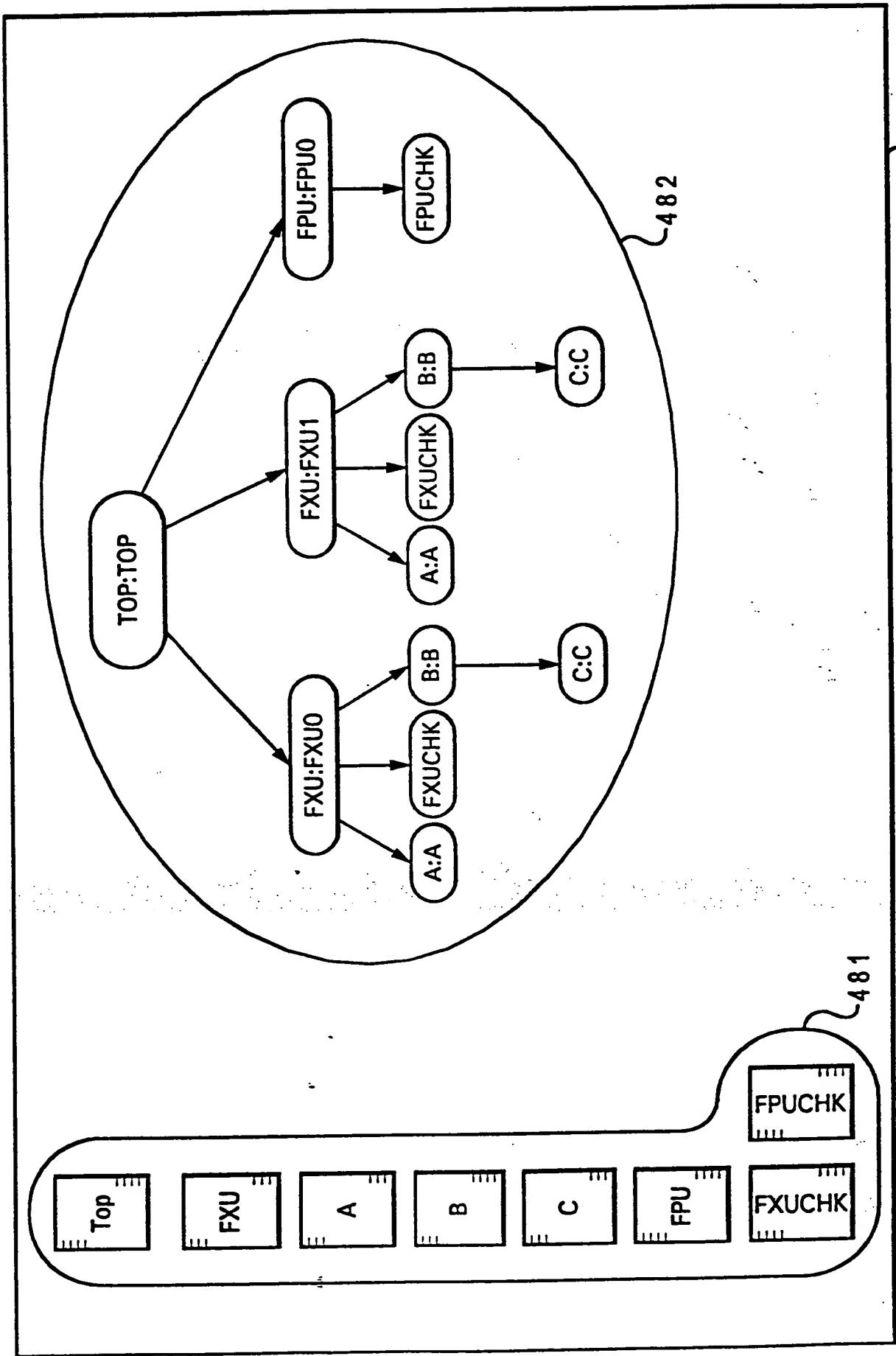


Fig. 4E

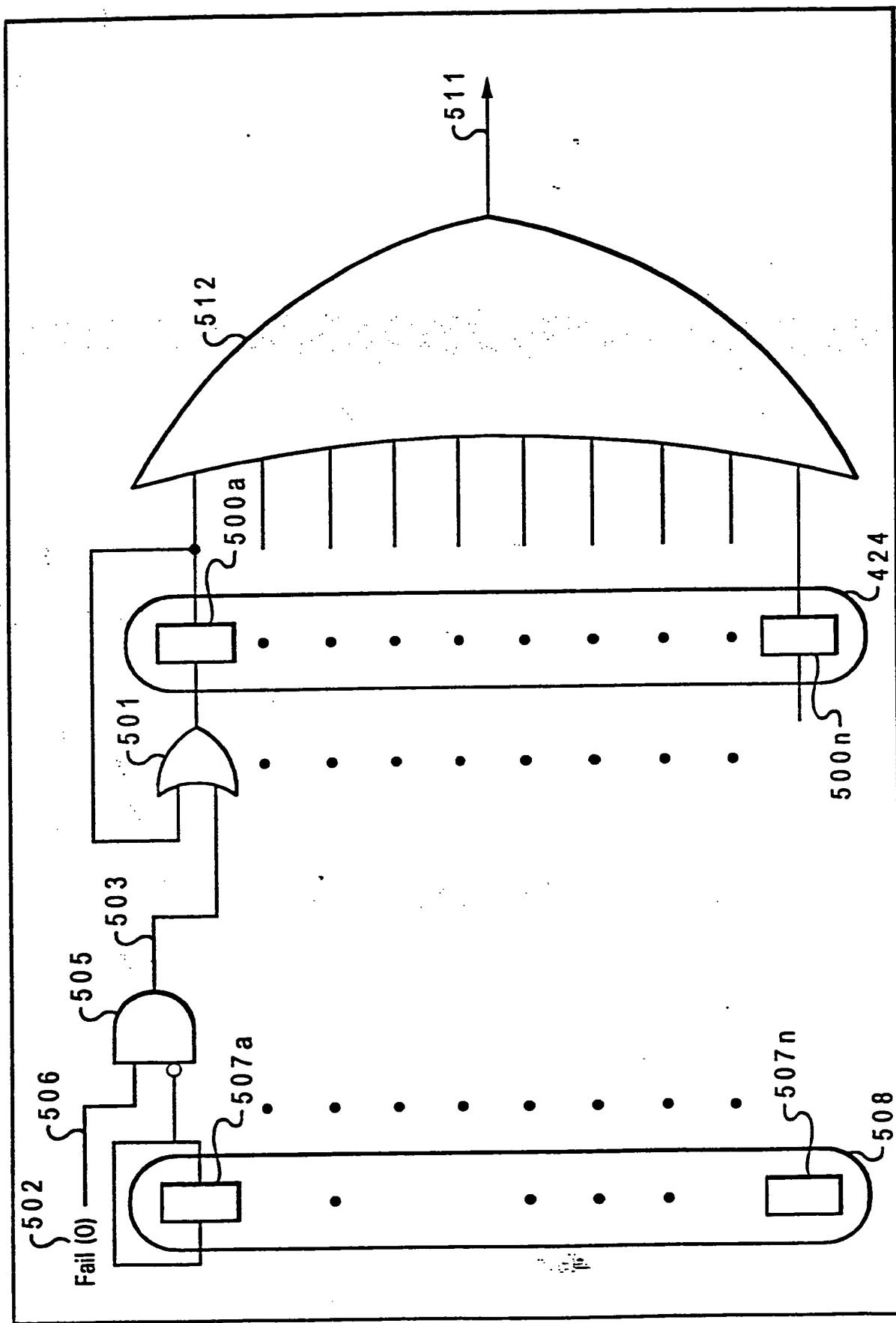


Fig. 5A

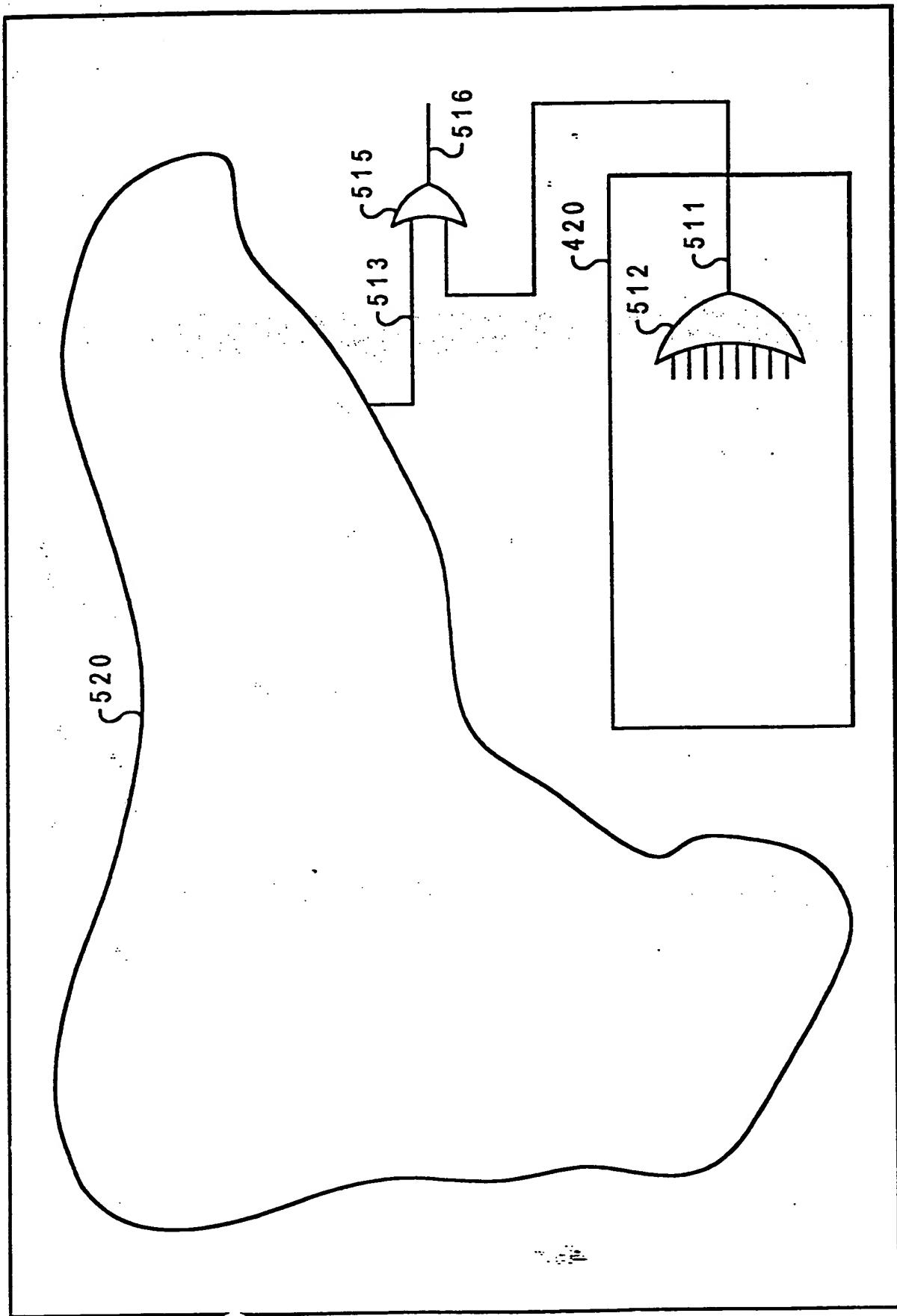


Fig. 5B

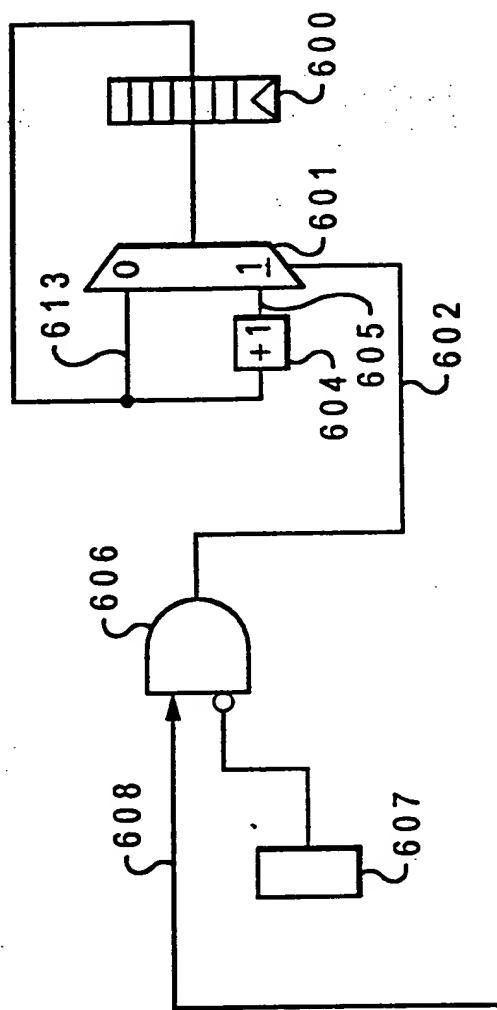


Fig. 6A

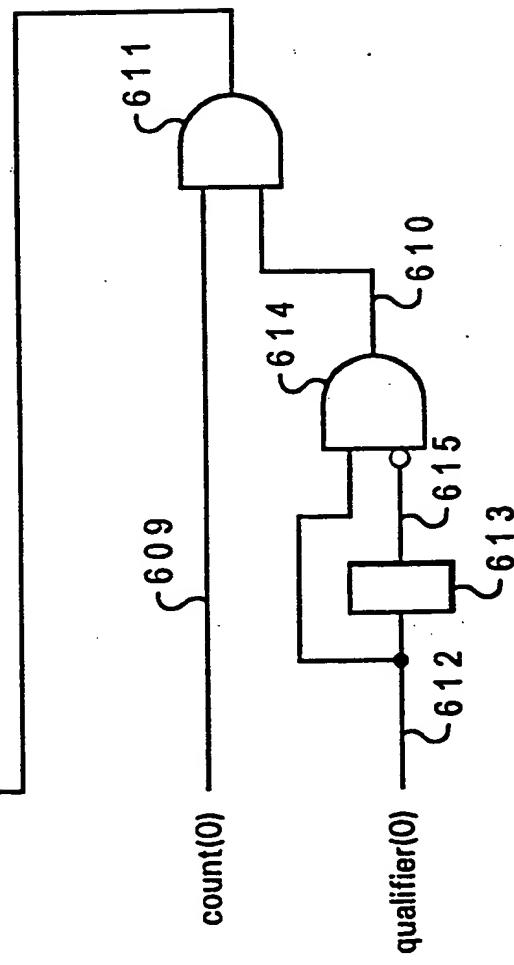
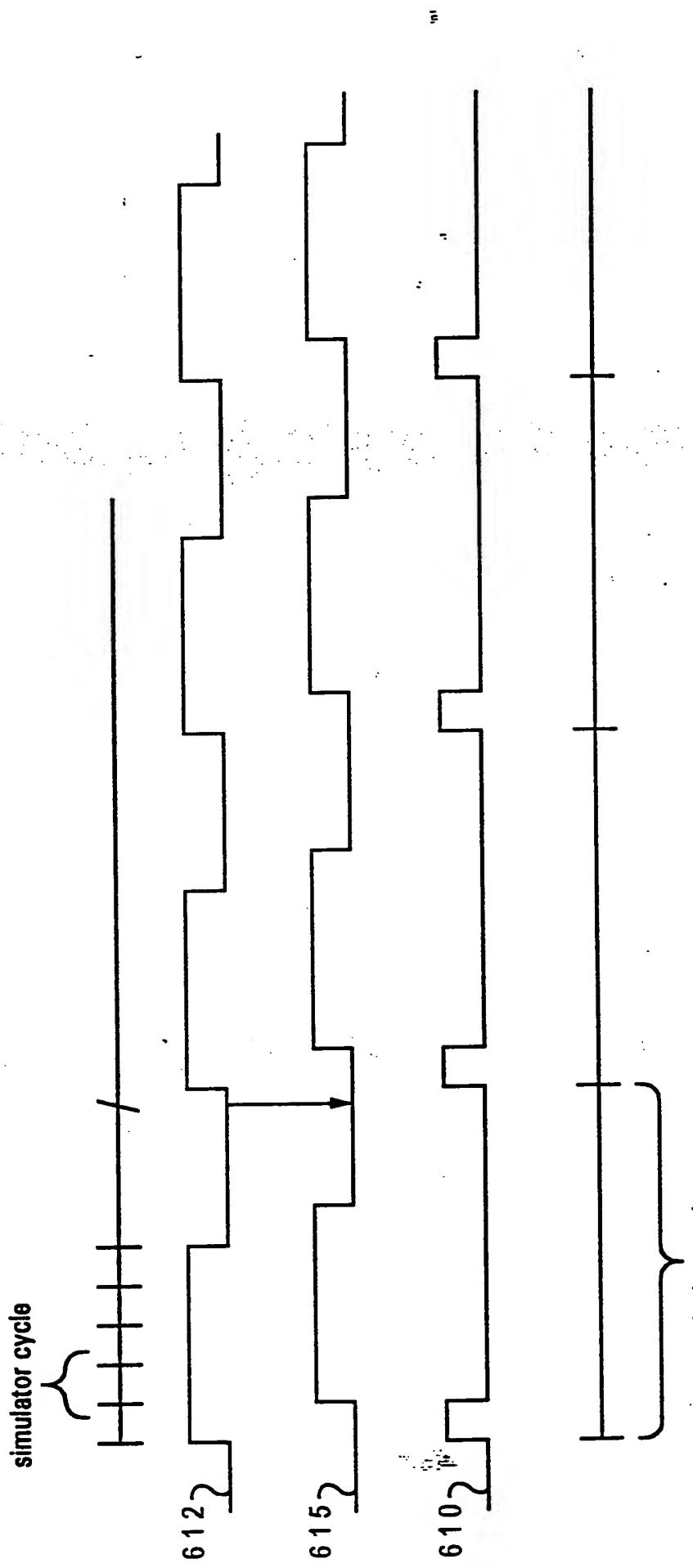


Fig. 6B



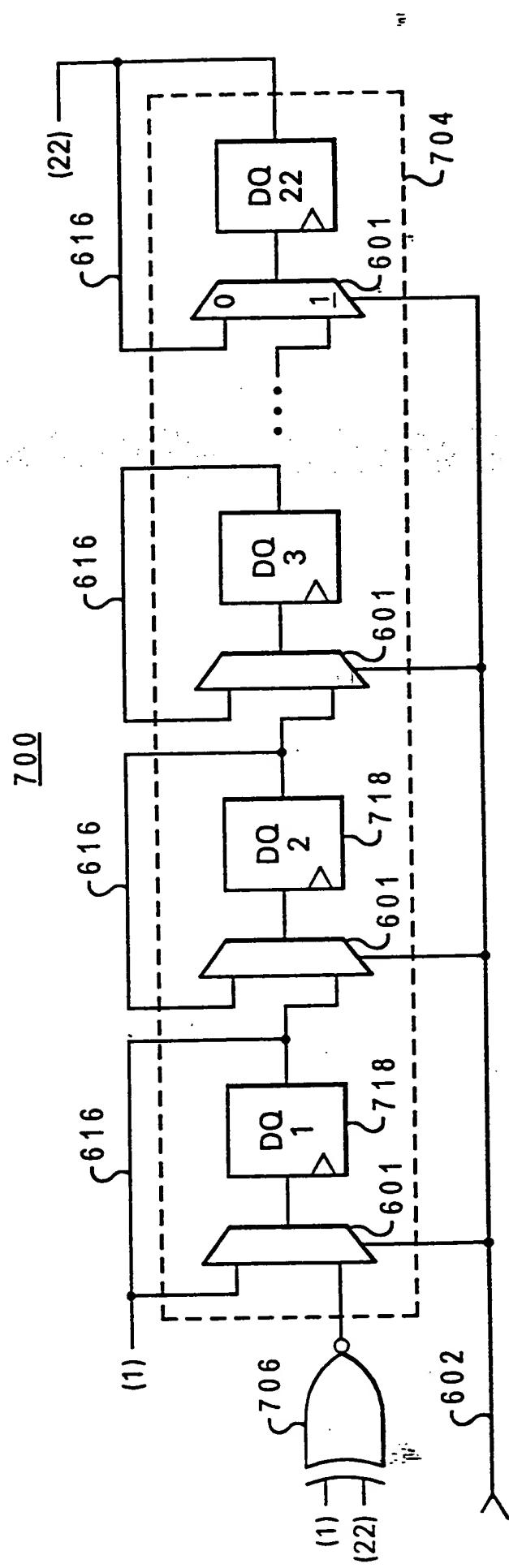


Fig. 7

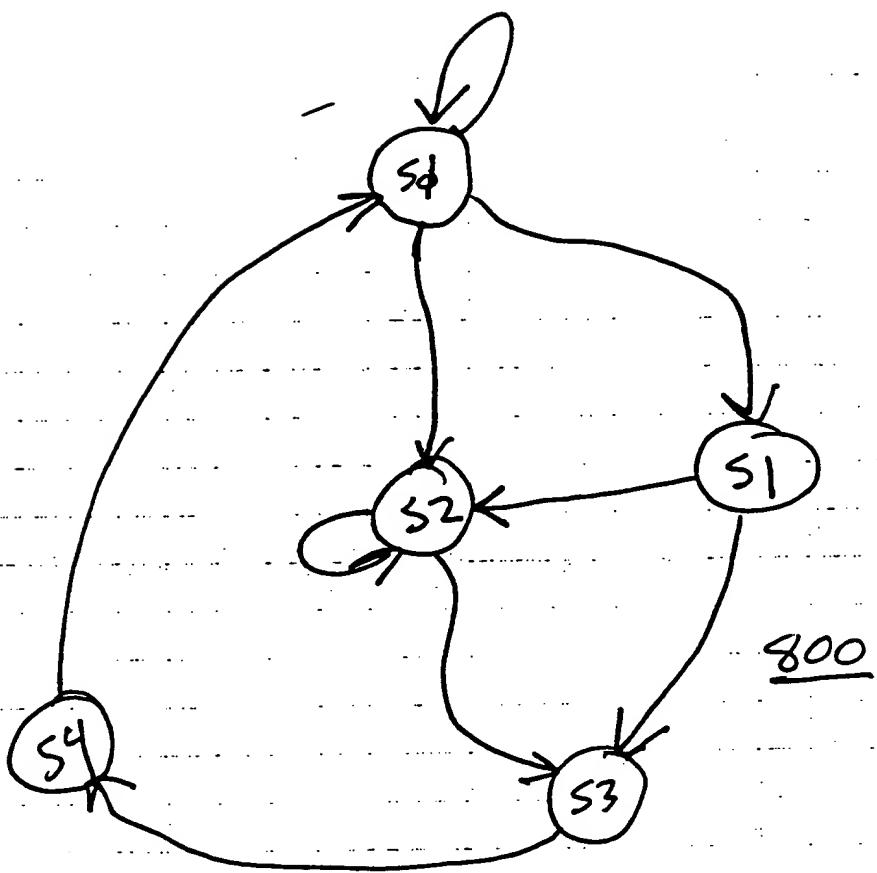


FIG. 8

(Prior Ant)

entity  $\text{Fsm}:\text{Fsm}$

850

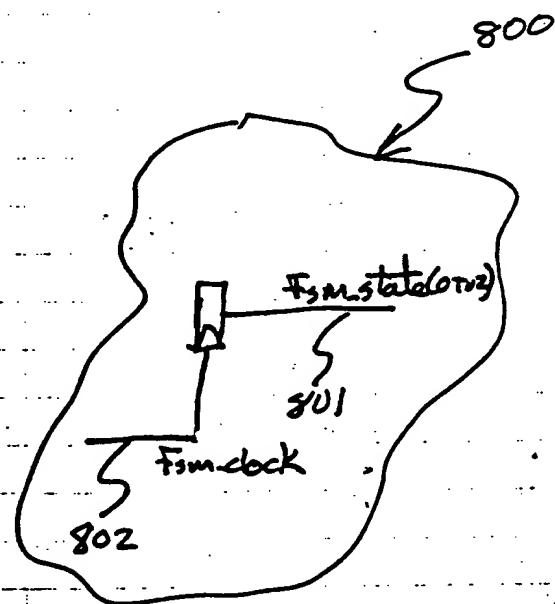


FIG. 8A  
(Prior Art)

entity FGM I3

PORT (

.... ports for entity from ...

j

## Architecture form of FSM IS

BEGUN

.... HDL code for Fsm and rest of the entity. ....

fsm-state(0 to 2) <-- ... signal 801 ...

853 859 854 855 856 857

658 ~~Aug~~ - ?! end Fsmj

END;

FIG. 8B

entity FSM:FSM

850

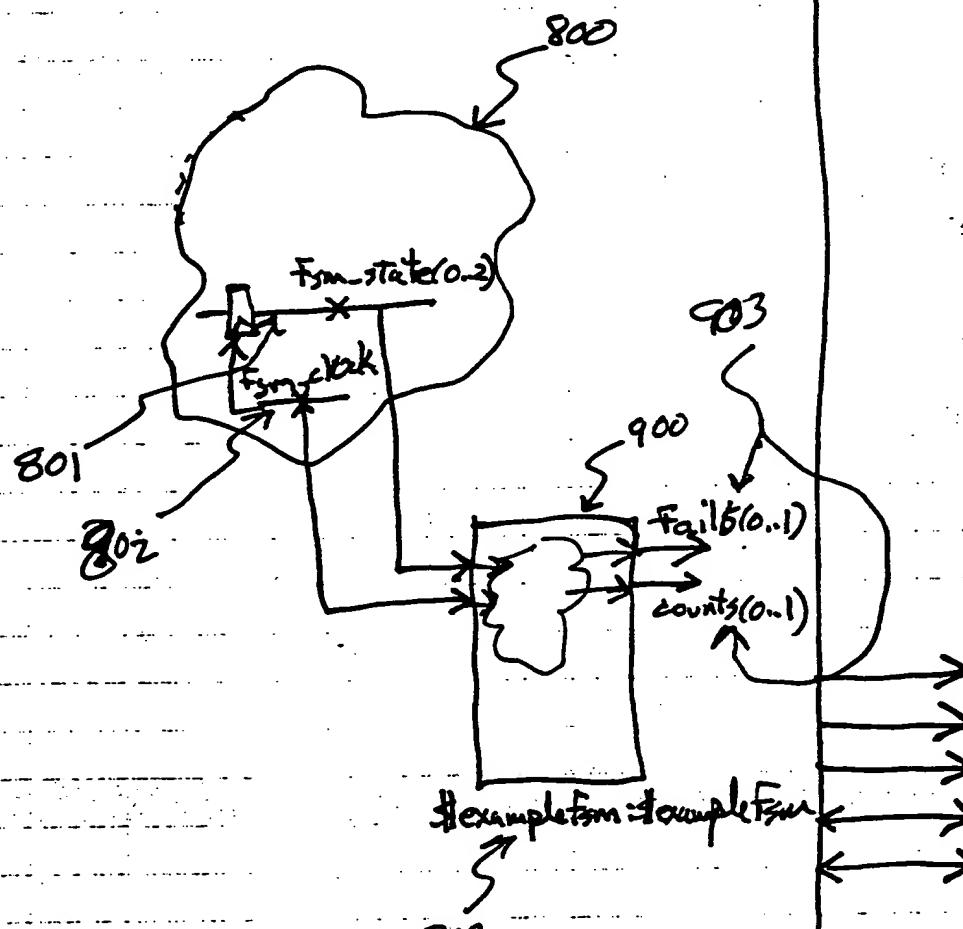


FIG. 9

TOP, TOP

X:111  
1010a

B3:63  
1012a

2:2  
1014a

2:87  
1018a

X:112  
1010b

B7:83  
1012b

2:2  
1014b

2:82  
1018b

Y:1Y  
1020

B4:84  
1022

2:2  
1016c

2:12  
1018c

FIG. 10A

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